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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,673	12/17/2003	Ryusuke Sahara	520.43336X00	4121

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EXAMINER	
CHANG, DANIEL D	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,673	SAHARA ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation, "signal paths disposed on both sides are respectively set to a fixed potential" in claim 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: On page 4, line 22, "Fig. 8 is a waveform diagram" should be changed to "Figs. 8A-8D are waveform diagrams".

Appropriate correction is required.

Claim Objections

Claims 5 and 6 are objected to because of the following informalities: the recitation, "an AC test" needs to be spelled out since it is not clear what it refers to. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

On line 4, the recitation, "the two of the first signal path" lacks antecedent basis.

On line 6, the recitation, "signal paths disposed on both sides" is not clear what it refers to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipate by Lackey (US 5,783,960).

Regarding claim 1, Lackey discloses, in Figs. 1-4, a semiconductor integrated circuit device comprising:

first signal path (one of trees 18-26) that transfers a first signal supplied from outside (outside of Clock Powering Logic 46);

a second signal path (one of trees 18-26) that transfers a second signal supplied from outside (outside of Clock Powering Logic 46); and

at least one pulse generator (28) that forms a first pulse (42 or 44 in Fig. 3) corresponding to a difference in phase between the first signal and the second signal in response to the first signal and the second signal,

wherein the number of buffer stages provided in the first signal path and the second signal path is greater than (inherent for TREES 18-26) the number of combination circuit stages provided in the pulse generator (see Fig. 2).

Regarding claim 2, Lackey discloses, in Figs. 1-4, a semiconductor integrated circuit device comprising:

first signal path (one of trees 18-26) that transfers a first signal supplied from outside (outside of Clock Powering Logic 46);

a second signal path (one of trees 18-26) that transfers a second signal supplied from outside (outside of Clock Powering Logic 46); and

at least one pulse generator (28) that forms a first pulse (42 or 44 in Fig. 3) corresponding to a difference in phase between the first signal and the second signal in response to the first signal and the second signal,

wherein a whole wiring length of the first signal path and the second signal path is longer than a wiring length between the pulse generator and a circuit to which the pulse is transferred (inherent since trees have more buffers and longer lines).

Regarding claim 3, Lackey discloses, in Figs. 1-4, a semiconductor integrated circuit device comprising:

first signal path (one of trees 18-26) that transfers a first signal supplied from outside (outside of Clock Powering Logic 46);

a second signal path (one of trees 18-26) that transfers a second signal supplied from outside (outside of Clock Powering Logic 46); and

at least one pulse generator (28) that forms a first pulse (40, 42 or 44, see Figs. 1 and 3) corresponding to a difference in phase between the first signal and the second signal in response to the first signal and the second signal,

wherein a rising time up to full amplitude at any one of buffers in the first signal path and the second signal path is longer than a pulse width of the first pulse (inherent since trees have more buffers and longer lines).

Regarding claim 4, Lackey discloses, in Figs. 1-4, a third signal path (one of trees 18-26) supplied with a third signal from an external terminal (outside of Clock Powering Logic 46), wherein the pulse generator forms a second pulse (40, 42 or 44, see Figs. 1 and 3) corresponding to a difference in phase between the second signal and the third signal.

Regarding claim 5, Lackey discloses, in Fig. 4, combination circuits (82) and LSSD type flip-flops (80, 84) respectively provided on the input and output sides of the combination circuits, wherein the first pulse and the second pulse are used in an AC test operation of said each combination circuit (col. 2, lines 56+).

Regarding claim 6, Lackey discloses, in Figs. 1-4, that the first signal path, the second signal path and the third signal path extend in a direction parallel to each other and are placed adjacent to each other (see 18-26 in Fig. 1), and includes the same number of buffer stages (inherent), and the pulse generator outputs clock the first pulse and second pulse an AC test (col. 1, lines 27+) said each combination circuit, and clock pulses for serially transferring a test input signal and a test output signal to said each LSSD type flip-flop a test mode (col. 1, lines 27+), and outputs any one of the first through third signals as clock pulse upon a normal operation (col. 1, lines 27+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lackey (US 5,783,960).

Lackey discloses all the claimed elements and means as discussed above but does not disclose that each of elements that constitute the buffers comprises a MOSFET having a metal gate structure.

However, it is well known in the art that the MOSFET having a metal gate structure are widely and commonly used for high-speed switching applications and to reduce the resistance value of the gate electrode. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided the circuit of Lackey with well known MOSFET having a metal gate structure because of its high speed operation and to reduce the resistance value of the gate electrode. It is matter of engineering choice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER